

Aug 25/04

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DBs:	USPTO:US PTO/USPTO, EPO: EPO, DIVERVENT:ICM_TDB			
Default operator: OR		<input type="checkbox"/> Plural <input type="checkbox"/> Highlight all the terms initially		
12 and 5				

#	Invantor	Document	Issue Date	Type	Current Status	XN	Review	S	C	F	Y	Z	Image	Date	P
1	<input type="checkbox"/> Inagawa, Hi	US 200201120020	2	Insulated gate type semiconductor device an	438/270-257/330	<input type="checkbox"/>	US 200201								
2	<input type="checkbox"/> Noble, Wend	US 200100220011	2	Circuits and methods using vertical complem	257/330	<input type="checkbox"/>	US 200100								
3	<input type="checkbox"/> Noble, Wend	US 677774420040	2	Circuits and methods using vertical, complem	257/330-438/199	<input type="checkbox"/>	US 677774								
4	<input type="checkbox"/> Madson, Gor	US 657695420030	1	Trench MOSFET formed using selective epit	257/330-257/2141	<input type="checkbox"/>	US 657695								
5	<input type="checkbox"/> Furukawa, T	US 644080120020	7	Structure for folded architecture pillar mem	438/272-257/302	<input type="checkbox"/>	US 644080								
6	<input type="checkbox"/> Noble, Wend	US 624277520010	2	Circuits and methods using vertical complem	257/330-257/351	<input type="checkbox"/>	US 624277								
7	<input type="checkbox"/> Furukawa, T	US 611472520000	7	Structure for folded architecture pillar mem	257/330-257/286	<input type="checkbox"/>	US 611472								
8	<input type="checkbox"/> Burns, Jr, Si	US 599050919991	6	2F square memory cell for gigabit memory ap	257/296-257/316	<input type="checkbox"/>	US 599050								
9	<input type="checkbox"/> Park, Kyuch	US 581255919970	1	Semiconductor device having pillar shaped tr	257/302-257/301	<input type="checkbox"/>	US 581255								
10	<input type="checkbox"/> Shah, Pradee	US 550854418960	1	Three dimensional FAMOS memory devices	257/316-257/321	<input type="checkbox"/>	US 550854								

/inc /desc /sc /nm

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